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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,587	12/28/2001	Guy L. Steele JR.	6502.0369	2874

60667 7590 12/27/2006

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	12/27/2006	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/035,587
Filing Date: December 28, 2001
Appellant(s): STEELE, GUY L.

Nathan A. Sloan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 07, 2006 appealing from the Office action mailed May 31, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The Appeal of U.S. Patent Application No. 10/035,579.

The Appeal of U.S. Patent Application No. 10/035,747.

The Appeal of U.S. Patent Application No. 10/035,584.

The Appeal of U.S. Patent Application No. 10/035,595.

The Appeal of U.S. Patent Application No. 10/035,647.

The Appeal of U.S. Patent Application No. 10/035,580.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-3 and 5-47.

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The modifications are as follows:

Claims 1-3 and 5-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

It is noted that upon further review of the claims and the Huang et al. patent, it has been determined that Huang et al. anticipates the invention as recited in claims 1-3 and 5-47 currently under appeal. The grounds of rejection section of this Examiner's Answer sets forth the modified rejection of claims 1-3 and 5-47 in view of Huang et al.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,995,991	HUANG ET AL.	11-1999
6,009,511	LYNCH ET AL.	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

(10) ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

B. Claims 1-3 and 5-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

As per independent claim 1, Huang et al disclose, e.g., see **Fig. 4**, the invention, **arithmetic calculation circuit (100)**, substantially as claimed, including: **X and Y operand registers 116 & 118; arithmetic section 114 and special operand generator 122**. Huang et al's disclosed X and Y operand registers each includes a special operand indicator (116-2 and 118-2) which is stored as special operand of a predetermined set of special operands. It is noted that although Huang et al do not refer to an "analyzer circuit" per se, Huang et al.'s device is configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand, similar to the function of the claimed analyzer circuit, thus Huang et al.'s

arithmetic **calculation circuit (100)** having special operand indicator in each operand register corresponds to the "analyzer circuit" as claimed.

As per dependent claim 2, the claim adds "wherein at least one of the plurality of operands is a floating point operand". Huang et al's device is a floating point device.

As per dependent claim 3, the claim adds "further comprising one or more **operand buffers**. The memory (register file) 112 in Huang's Fig. 4 corresponds to the claimed "operand buffer", since a buffer is nothing more than a storage for temporary storing desired data, and Huang's disclosed register file 112 clearly store operands at least temporarily.

As per dependent claims 5-14 and 17, the claims add the detail "formats", "flags", "status". These features are inherent in special floating point number disclosed in Huang.

As per dependent claim 15, the claim adds "wherein the accumulated result represents information from one of the plurality of operands that has a larger fraction field". As per dependent claim 16, the claim adds "wherein the a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands". These features are inherent in Huang's disclosed floating point operations.

Due to the similarity of claims 18-47 to claims 1-3 and 5-17, they are rejected under a similar rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

C. Claims 1-3 and 5-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch et al .

As per independent claim 1, Lynch et al disclose, e.g., see **Fig. 4**, the invention, **floating point unit (36)**, substantially as claimed, including: **Register Stack (84) and FPU Core (94)**. Although Lynch et al do not explicitly describe an "analyzer circuit" per se, Lynch's disclosed floating point system is configured to determine a **first status** of a first floating point operand and a **second status** of a second floating point operand ("whether each floating point operand is a normal floating point number or a special floating point number" in abstract, lines 1-7), as recited in the instant claim, thus Lynch's

floating point unit in Lynch's system inherently includes an analyzer circuit for performing the determination. Lynch et al. do not explicitly disclose that the resulting status tag is embedded within the resulting floating point operand, as claimed. Lynch et al. do disclose in Fig. 6 that the register stack (84) for storing operand includes result operand having a tag field (89) within the operand for storing appended tag values (see the bridging paragraph of cols. 15 and 16). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to store the floating point result with its tag as a resulting operand in Lynch's register stack (84) in order to quickly determine its status in subsequent operations.

As per dependent claim 2, the claim adds "wherein at least one of the plurality of operands is a floating point operand". Lynch et al's device is a floating point device.

As per dependent claim 3, the claim adds "further comprising one or more **operand buffers**. The "operand buffer" feature is well known in the art for temporary storing desired data. Therefore, including buffers in Lynch's floating point system would have been obvious to one of ordinary skill in the art in order to avoid error due to logic switching of operands.

As per dependent claims 5-14 and 17, the claims add the detail "formats", "flags", "status". These features are inherent formats in special floating point number disclosed by Lynch.

As per dependent claim 15, the claim adds "wherein the accumulated result represents information from one of the plurality of operands that has a larger fraction

field". As per dependent claim 16, the claim adds "wherein the a sign bit in the accumulated result is a logical OR of sign bits in the plurality of operands".

Due to the similarity of claims 18-47 to claims 1-3 and 5-17, they are rejected under a similar rationale.

(11) Response to Argument

Appellant's arguments filed April 07, 2006 have been fully considered but they are not persuasive. Appellant argues that:

B1. Claims 1-3 and 5-47 patentably distinguish from Huang

"Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example, 'an analysis circuit that receives a plurality of operands each of which having encoded status flag information, the analysis circuit being operative to analyze the plurality of operands and to provide an indication of one or more predetermined formats in which the plurality of operands are represented' (emphasis added)...

First, the Examiner has not identified specific teachings in Huang which correspond to the Examiner's coined term 'special operand indicator.' The Examiner has also not explained how this term relates to, for example, the claimed 'plurality of operands each of which having encoded status flag information" as recited by claim 1 (emphasis added).

Second, even assuming the Examiner's coined term "special operand indicator" refers to a tag value of Huang (Huang, FIG. 4, 116-2), Huang's teaching of a "tag value" does not constitute a teaching or suggestion of a "plurality of operands each of which having encoded status flag information" (emphasis added) as recited by claim 1...

Moreover, independent claim 1 recites a combination also including, for example, 'a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands' (emphasis added). Huang does not teach or suggest at least this additional element. The Examiner has not identified any portions of Huang which provide a teaching or suggestion of a 'result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands,' as recited by claim 1 (emphasis added). See Office Action mailed October 22, 2004 at pp. 3-4. For at least this reason, the Examiner's rejection is improper...

First, the Examiner's assertion is directed to a special operand indicator 'in each operand register.' Id. (emphasis added). Discussion of 'a special operand indicator in a each operand register' however, does not constitute motivation for a 'plurality of operands each of which having encoded status flag information,' as recited by claim 1 (emphasis added). Discussion of 'a special operand indicator in a each operand register,' also does not constitute motivation for a 'result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents

a value and combines the encoded status flag information from each of the plurality of operands,' as recited by claim 1 (emphasis added).

Second, the Examiner uses impermissible hindsight in reconstructing Appellant's claimed invention. A determination of obviousness must 'take into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and ... [must] not include knowledge gleaned only from' Appellant's disclosure. In re McLaughlin, 443 F.2d 1392, 1395, 170 USPQ 209, 212 (CCPA 1971) (emphasis added). As discussed above, the Examiner concedes that Huang does not teach determining a 'plurality of operands each of which having encoded status flag information.' Office Action mailed October 22, 2004 at p. 3. No other reference is cited to cure this deficiency. Therefore, the Examiner's determination of obviousness could not have been founded on knowledge within the level of skill in the art when Appellant's claimed invention was made. Such determination instead impermissibly relied on hindsight reasoning by looking to Appellant's specification. For at least this additional reason, there is no motivation to modify Huang to arrive at Appellant's invention as recited by claim 1."

B2. Claims 3, 5-17, 20-32 and 35-47 patentably distinguish from Huang

"Huang does not disclose each and every element of dependent claims 3, 5-17, 20-32, and 35-47. In fact, the Examiner has not addressed any of the elements recited by dependent claims 3, 5-17, 20-32, and 35-47, other than to say that these features are "well known" and "obvious." See Office Action mailed October 22, 2004 at p. 4.

These bare assertions fail to meet the requirement that the prior art teach or suggest each and every element of claims 3, 5-17, 20-32, and 35-47. Moreover, the Examiner has not provided any motivation to make the alleged design choice modification. Id."

C1. Claims 1-3 and 5-47 patentably distinguish from Lynch

"[f]irst, the Examiner has not explained how Lynch's 'tag values' relate to, for example, 'a plurality of operands each of which having encoded status flag information,' as recited by claim 1. Even if Lynch's tag value were to constitute the claimed 'status,' (which Appellant does not concede) the tag value of Lynch is not 'encoded' within each operand, as recited by claim 1.

Fig. 4 of Lynch, which Appellant reproduces below, clearly illustrates that Tag Field 89 (alleged status) and Reg Field 87 (operand) are separate from each other and are stored within register stack 84...

Moreover, Lynch specifically states that element 84 is a register stack, not an operand. Lynch also states that register stack 84 contains a Reg Field 87 for storing an operand separate from a Tag Field 89 for storing a tag (alleged status). See Lynch, col. 15, lines 63-67. "Separate from" cannot constitute "encoded" within the operand, as recited by claim 1.

Moreover, independent claim 1 recites a combination including, for example, "a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands" (emphasis added). The Examiner

has not addressed this element or identified any specific teachings of Lynch which would allegedly teach or suggest 'a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands,' as recited by independent claim 1. See Office Action mailed October 22, 2004 at p. 5. For at least this reason, the Examiner's rejection is improper...

First, the Examiner's assertion is directed to determining "which floating point numbers are special floating point numbers and the type of special floating point number' (Office Action mailed October 22, 2004 at p. 5). However, such discussion of generally determining "which numbers are special floating point numbers" does not constitute motivation for "a plurality of operands each of which having encoded status flag information," as recited by claim 1 (emphasis added). The discussion of generally determining "which numbers are special floating point numbers" also does not constitute motivation for "a result assembler that receives the indication from the analysis circuit and assembles an accumulated result that represents a value and combines the encoded status flag information from each of the plurality of operands," as recited by claim 1 (emphasis added).

Second, Lynch's teaching that "a tag value is appended to each floating point number stored in a floating point register' (Lynch, col. 5, lines 44-45) directly teaches away from the claimed structure, which requires "a plurality of operands each of which having encoded status flag information" (emphasis added)."

C2. Claims 3, 5-17, 20-32 and 35-47 patentably distinguish from Lynch

"Lynch does not disclose each and every element of dependent claims 3, 5-17, 20-32, and 35-47. As with Huang, discussed above, the Examiner has not addressed any of the elements recited by dependent claims 3, 5-17, 20-32, and 35-47, other than to say that '[t]hese features are obvious' and 'well known.' See Office Action mailed October 22, 2004 at p. 5. This bare assertion meets neither the requirement for showing how Lynch allegedly teaches or suggests each and every element of dependent claims 3, 5-17, 20-32, and 35-47, nor the requirement to establish motivation to make the alleged modification. Id. Accordingly, no prima facie case of obviousness has been established with respect to claims 3, 5-17, 20-32, and 35-47. Appellant requests that the Board overturn the Examiner's rejection."

With respect to the arguments, the examiner carefully reviews Appellant's specification, drawings, claimed invention and the applied references.

B1. Claims 1-3 and 5-47

It is noted that "X" SPECIAL OPERAND INDICATOR (x_tag) and "Y" SPECIAL OPERAND INDICATOR (y_tag) of Fig. 4 are equivalent to the claimed "determine a **first status** ... and **second status**" feature (e.g., see Abstract, lines 7-10; and claim 1, para. (a) for detail of the tag). According to Fig. 4, "X" (116-1) and "x_tag" (116-2) are belonged to a "X" register (116). In col. 6, lines 64-65, Huang specifically states "**X** and Y **operand** registers 116 and 118 ..." Therefore, it is clearly that Huang's teaching of a

"tag value" does constitute a teaching data within the floating point **operand** as claimed. Although the tag generator (150) to generate the tag value separately from the output of arithmetic section (114), the examiner believes that the resulting status "tag value" embedded within the "resulting floating point operand". It is noted that the format [resulting status embedded within the resulting floating point operand] of **stored data** in the MEMORY (REGISTER FILE) 112 is the **same as** the format [status data within the floating point operand] of **data transferred** to "X" or "Y" register because the **read out / write in data** is usually unchanged. Therefore, the **stored** "resulting floating point operand" includes the "resulting status" as claimed.

B2. Claims 3, 5-17, 20-32 and 35-47

It is noted that Huang does teach claimed "status" information, e.g., zero, overflow, underflow, etc. status flags (col. 7, lines 20-23); Not a number, etc. (TABLE 1). Also, Huang' s claim 3 discloses "positive infinity" & "negative infinity" features as Appellant's claim 14.

C1. Claims 1-3 and 5-47

It is noted that the "Tag Field" (89) contains the "status" information of each register of Register Stack (84), e.g., see Abstract. According to Fig. 4, "Reg Field" (87) and "Tag Field" (89) are belonged to Register Stack (84). Therefore, it is clearly that Lynch's teaching of a "tag value" does constitute a teaching data within the floating point **operand** as claimed. Although the tag value is appended to each floating point number

stored in a floating point register, the examiner interprets the floating point register as a operand. Therefore, that the resulting status "tag value" embedded within the "resulting floating point operand".

C2. Claims 3, 5-17, 20-32 and 35-47

It is to be noted that Lynch teaches the claimed "status" information, e.g.,"[t]ypes of special floating point numbers include zero, +infinity, -infinity and NaNs" (col. 17, lines 6-7) and Fig. 5. In col. 18, first complete paragraph, Lynch discloses "+infinity" & "-infinity" features as Appellant's claim 14.

(12) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(13) For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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